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IT8711F

Low Pin Count Input / Output (LPC I/O)

Preliminary Programming Guide V0.1

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1. Overview

The IT8711F is a LPC Interface based highly integrated Super I/O. The IT8711F provides the most commonly used legacy Super I/O functionality The device's LPC interfa ce complies with Intel 'LPC Interface Specification Rev. 1.01". The IT8711F meets the "Microsoft ® PC98/PC99/PC2001 System Design Guide" requirements and is ACPI compliant.

Features include one high-performance 2.88MB floppy disk controller, with digital data separator, supporting one 360K/720K/1.2M/1.44M/2.88M floppy disk drive. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V.1.7 and EPP V.1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and support SIR. The Smart Card Interface is internally connected to UART2. The Keyboard Controller, Consumer IR, MIDI and Game Port are also supported.

These 9 logical devices can be individually enabled or disabled via software configuration registers. The IT8711F utilizes power-efficient circuitry to reduce power consumption. Once a logical device is disabled, the inputs are gated inhibit, the outputs are TRI-STATE and the input clock is disabled. The IT8711F requires a single 24/48 MHz clock input and operates with a +3.3V power supply.

The IT8711F is available in 100-pin QFP (Quad Flat Package).

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www.iteusa.com   *Dec. 27, 2001*
Specifications subject to Change without Notice

2. Block Diagram

3. Pin Configuration

IT8711F
100-QFP

Top View

Left side (pins 1–30):
1 DCD2#/GP62
2 SIN2/GP63
3 GND
4 RI2#/GP10
5 CTS2#/GP11
6 DTR2#/GP12
7 RTS2#/GP13
8 DSR2#/GP14
9 SOUT2/GP15
10 GA20/GP16
11 KRST#/GP17
12 KCLK/GP20
13 KDAT/GP21
14 MCLK/GP22
15 MDAT/GP23
16 PWBTIN#/GP24
17 PWBTOUT#/GP25
18 SLPSX#/GP26
19 PWRCTL#/GP27
20 VID0/GP30
21 VID1/GP31
22 VID2/GP32
23 VID3/GP33
24 VID4/GP34
25 GP35*
26 GP36*
27 VCCH
28 GND
29 VBAT
30 KBLK#/CIRTX/GP40*

Top (pins 100–81):
100 JVR/GP61
99 JACX/GP50
98 JACY/GP51
97 JBCX/GP52
96 JBCY/GP53
95 JAB1/GP54
94 JAB2/GP55
93 JBB1/GP56
92 JBB2/GP57
91 VCC
90 DSR1#
89 SOUT1/JP3
88 SIN1
87 RTS1#/JP2
86 DTR1#/JP1
85 DCD1#
84 RI1#
83 CTS1#
82 PD7
81 PD6

Bottom (pins 31–50):
31 CIRRX/GP41*
32 IRTX/GP42*
33 IRRX/GP43*
34 PME#
35 SCPSNT#/GP44
36 SCRST/GP45
37 SCPWR/GP46
38 SCCLK/GP47
39 SCIO/GP60
40 LDRQ#
41 LFRAME#
42 LRESET#
43 SERIRQ
44 LAD0
45 LAD1
46 LAD2
47 LAD3
48 PCICLK
49 DENSEL#
50 MTRA#

Right side (pins 80–51):
80 PD5
79 PD4
78 GND
77 PD3
76 PD2
75 PD1
74 PD0
73 STB#
72 AFD#
71 ERR#
70 INIT#
69 SLIN#
68 BUSY
67 ACK#
66 SLCT
65 PE
64 WPT#
63 INDEX#
62 TRK0#
61 DSKCHG#
60 RDATA#
59 DIR#
58 WGATE#
57 HDSEL#
56 STEP#
55 WDATA#
54 VCC
53 GND
52 CLKIN
51 DRVA#

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4. Programming Sequence and Flow Charts

4.1   Configuring Sequence Description
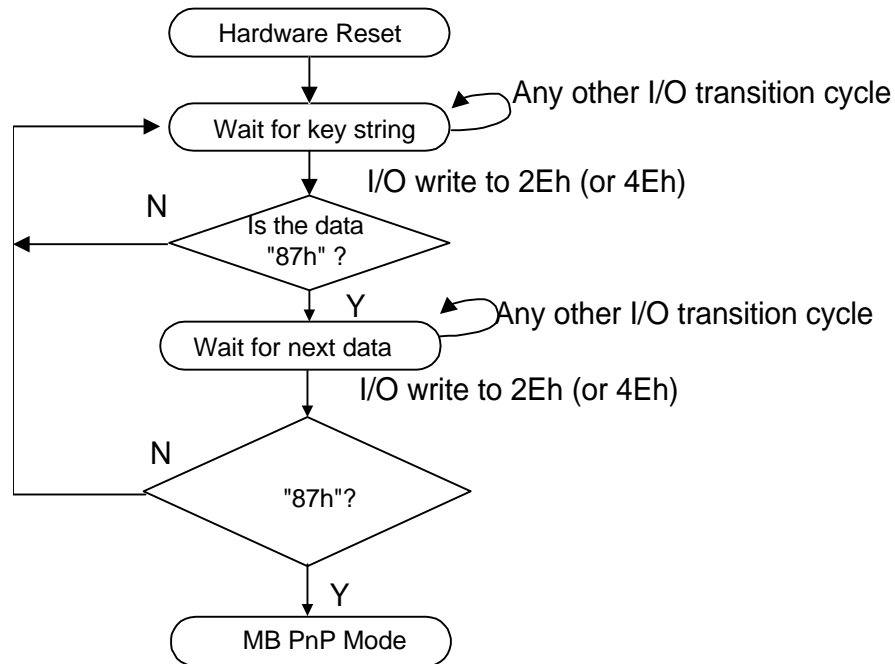
Figure 4-1. Enter the MB PnP Mode Flow Chart

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 2 specific I/O write operations (87h) must be performed during the "Wait for key" state. The addresses of the configuration Index/Data register pair are determined by the power-on strapping of pin 89 (JP3). 2Eh/2Fh is selected when the power-on strapping value of this pin is high (internal pull-up resistor); 4Eh/4Fh is selected when the power-on strapping value of this pin is low (external pull-down resistor).

(2) Modifying the Data of the Registers

All configuration registers can be accessed after the MB PnP Mode is accessed. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exiting the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to "1" to exit the MB PnP Mode.

4.2   FDC (LDN=00h)

Table 4-1. FDC Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Go in Configuration
out 2e 87
out 2e 87

Set LDN=00h
out 2e 07
out 2f 00
Get FDC base address
out 2e 60
in 2 f
out 2e 61
in 2 f

Set FDC Command

Read, Write...
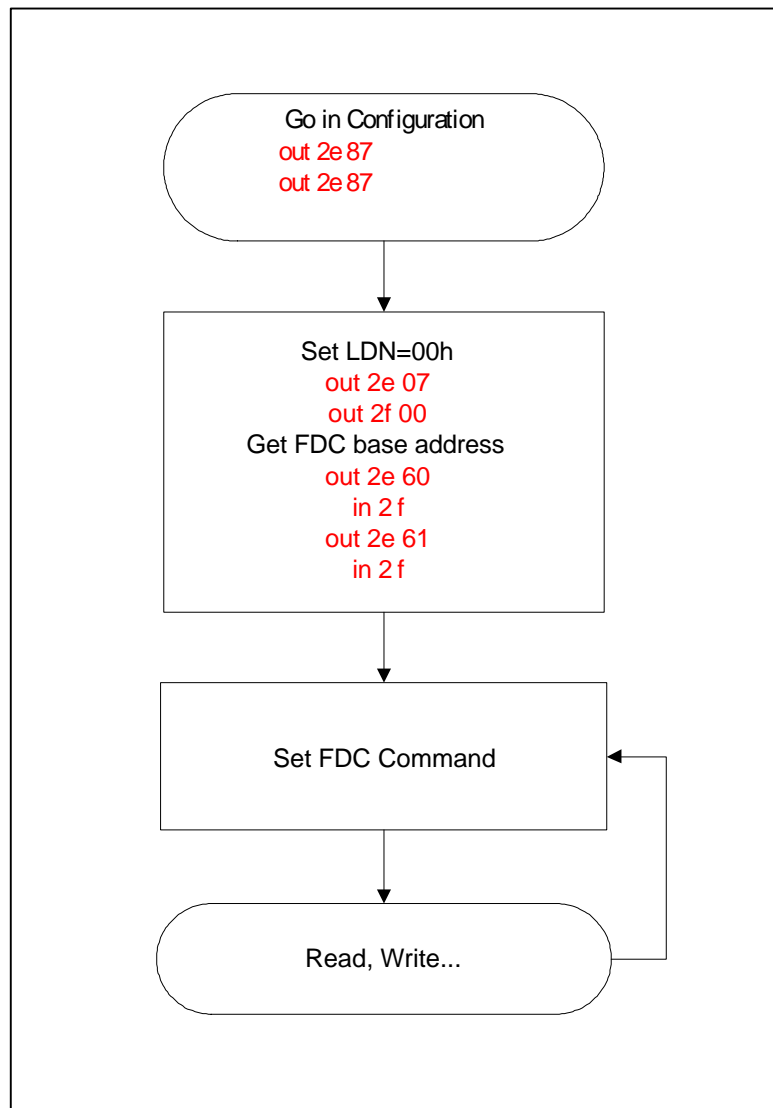
Figure 4-2. FDC Control Flow Chart

4.3 Serial Port 1 (LDN=01h)

Table 4-2. Serial Port 1 Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register
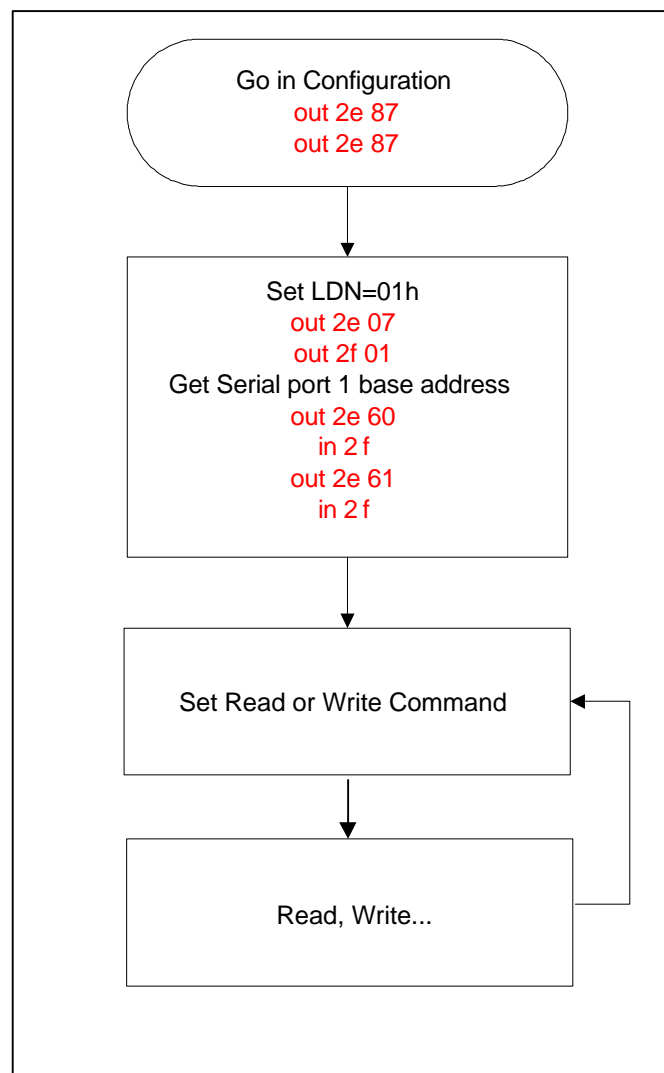
Figure 4-3. Serial Port Control Flow Chart

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4.4   Serial Port 2 (LDN=02h)

Table 4-3. Serial Port 2 Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	00h	Serial Port 2 Special Configuration Register 3
02h	F3h	R/W	7Fh	Serial Port 2 Special Configuration Register 4

4.4.1   Serial Port 2 Configuration Registers (LDN=02h)

4.4.1.1 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with '0h" for Base Addresses [15:12].
3-0	**Read/write**, mapped as Base Addresses [11:8].

4.4.1.2 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Addresses [7:3].
2-0	**Read only** as '000b."

4.4.1.3 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	Reserved with default '0h."
3-0	Select the interrupt level [Note1] for Serial Port 2.

Note 1: Interrupt level mapping

Fh-Dh: not valid
Ch: IRQ12
         .
         .
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

4.4.1.4 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-1	Reserved
0	**S2_IRQ_SHR (Serial Port 2 Interrupt Request Sharing)** 0: Normal (default). 1: Enable S2 IRQ sharing.

4.4.1.5 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	**IR_R2T_DLY (IR RX to TX Delay Mode)** 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. (default) 1: No transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	**IR_T2R_DLY (IR TX to RX Delay Mode)** 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 1: No transmission delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode (default).
5	**Reserved with default "0b"**
4	**HF_DLX (Half Duplex Enable)** 0: Full Duplex 1: Half Duplex (default)
3	Reserved with default '0b"
2-0	**S2_MOD (Serial Port 2 Mode)** 000: Standard (default) 001: IrDA SIR 010: ASKIR 100: Smart Card Reader (SCR) else: Reserved

4.4.1.6 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)

Bit	Description
7	**COM_PNP_EN** 0: Disable COM Port device Plug-and-Play operation (default). 1: Enable COM Port device Plug-and-Play operation.
6-5	Reserved
4	**PNP_ID** This bit is only available when bit 7=1. 0: PNP_ID Access mode (default). 1: Normal Plug-and-Play operation mode.
3	Reserved
2	**SCPWR_POR (SCPWR Polarity)** 0: Active low (default). 1: Active high.
1-0	**SCCLK_SEL1-0 (SCCLK Frequency Selection)** 00: Stop (default) 01: 3.5 MHz 10: 7.1 MHz 11: Special Frequency (96 MHz/SCDIV)

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4.4.1.7 Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)

Bit	Description
7	Reserved
6-0	SCDIV6-0 (SCCLK Special Divisor).

H/W Reset

IDLE — Waiting for ICC Insertion

Insert — Interrupt by UART sense PRESENT#

Power Up, Clock — Power up FET to 5V, then allow CLOCK out and Reset control, I/O in receive mode

Reset Card — Active level may differ

ATR — ICC responses to Answer-To-Reset within 400 - 40000 clo cycles of SCCLK, if N1, then RESET active high, if N2, the deactive

Decoding ATR — Driver translates the ATR

More Protocols — If no protocol is available, then treat as all default setting; If more protocols are available, the Driver can select a suital transfer protocol

PTS Request — IFD sends Protocol-Type-Selection request, and intends to change Xfer protocol

PTS Confirm — If the ICC accepts, then returns a confirm code

Change Protocol — Both IFD and ICC changed to new compromised protocol

Transfer — Begin to Xfer Data

Finish — For normal deactivation, the Driver controls the IFD to enter Deactive sequence

Clock Stop — Stop Clock

Power Down — Then power down FET

Emergency Remove

Remove

Protocol Error

If users remove the ICC at any time

Figure 4-4. Smart Card Operating Sequence Example

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```
┌─────────────────────────────────────────────────────────────────────┐
│                 ╭───────────────────────────────╮                      │
│                 │     Go in I/O configuration    │◀──────────┐         │
│                 │        OUT 2Eh, 87h, 87h       │           │         │
│                 │       Save original value      │           │         │
│                 ╰───────────────────────────────╯           │         │
│                                │                              │         │
│                 ┌───────────────────────────────┐           │         │
│                 │ Set LDN=01h or 02h to select UART1        │         │
│                 │ or UART2 Configuration Register│           │         │
│                 └───────────────────────────────┘           │         │
│                                │                              │         │
│                 ┌───────────────────────────────┐           │         │
│                 │     UART Function select:      │           │         │
│                 │        F1[2:0]=100b;           │           │         │
│                 │       Smart Card Reader         │           │         │
│                 └───────────────────────────────┘           │         │
│                                │                              │         │
│                 ┌───────────────────────────────┐           │         │
│                 │         F2[1:0]=01b;           │           │         │
│                 │    SCR_CLKSEL = 3.5 MHz        │           │         │
│                 └───────────────────────────────┘           │         │
│                                │                              │         │
│  BIOS Level     ┌───────────────────────────────┐           │         │
│                 │         F2[1:0]=01b;           │           │         │
│                 │    SCR_CLKSEL = 3.5 MHz        │           │         │
│                 └───────────────────────────────┘           │         │
└·················│··············································│·········┘
```

Go in I/O configuration
OUT 2Eh, 87h, 87h
Save original value

Set LDN=01h or 02h to select UART1
or UART2 Configuration Register

UART Function select:
F1[2:0]=100b;
Smart Card Reader

F2[1:0]=01b;
SCR_CLKSEL = 3.5 MHz

BIOS Level

F2[1:0]=01b;
SCR_CLKSEL = 3.5 MHz

Kernel mode driver

Set Baud rate = 9600
1. LCR[7] = 1b
2. DLL[7:0] = 0Ch
3. DLM[7:0] = 00h
4. LCR[7] = 0b

No parity; 8 data bits in width;
1 stop bit; LCR[3:0] = 0011b

Enable FIFO: write
FCR[0] = 1b
FCR[7:6] = 00b
IF FIFO is enabled,
read IIR[7:6] = 11b

Out2 enable;
Reset SCR and generate clock;
1. MCR [3] = 1b
2. MCR[1:0] = 00b
3. MCR[1:0] = 01b
4. MCR[1:0] = 11b

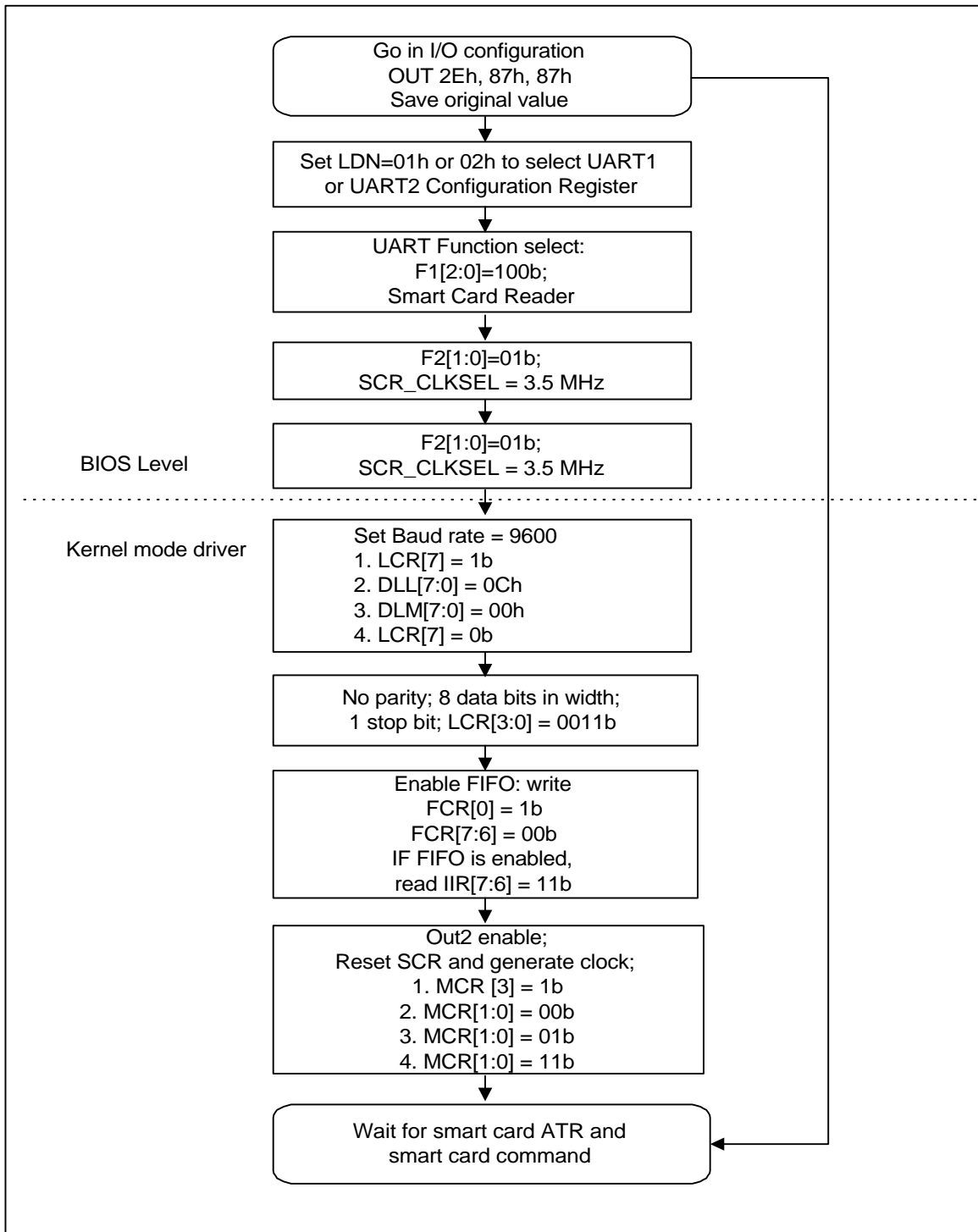Wait for smart card ATR and
smart card command

Figure 4-5. Flow Chart for IT8711F Smart Card Reader

4.5 Parallel Port (LDN=03h)

Table 4-4. Parallel Port Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	64h	R/W	00h	POST Data Port Base Address MSB Register
03h	65h	R/W	80h	POST Data Port Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select [Note1]
03h	F0h	R/W	03h [Note2]	Parallel Port Special Configuration Register

Note 1: When the ECP mode is not enabled, this register is **read only** as '04h", and cannot be written.
Note 2: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

4.5.1 SPP and EPP Modes

Table 4-5. Address Map and Bit Map for SPP and EPP Modes

Register	Address	R/W	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	RO	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

Table 4-6. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

Table 4-7. ECP Register Definitions

Name	Address	R/W	ECP Mode	Function
Data	Base 1 +000H	R/W	000-001	Data Register
EcpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
Dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	RO	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Table 4-8. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

```
                    ┌─────────────────────────┐
                    │   Go in Configuration   │
                    │       out 2e 87         │
                    │       out 2e 87         │
                    └─────────────────────────┘
                                 │
                    ┌─────────────────────────┐
                    │      Set LDN = 03h       │
                    │       out 2e 07          │
                    │       out 2f 03          │
                    │ Get Parallel Port base   │
                    │       address            │
                    │       out 2e 60          │
                    │         in 2f            │
                    │       out 2e 61          │
                    │         in 2f            │
                    └─────────────────────────┘
```

Set SPP Mode
out 2e f0
out 2f 00

Select SPP, EPP or ECP Mode?

Select ECP Mode
out 2e f 0
out 2f 02
Set DMA 3
out 2e 74
out 2f 03

Set EPP Mode
out 2e f0
out 2f 01

Read, Write...
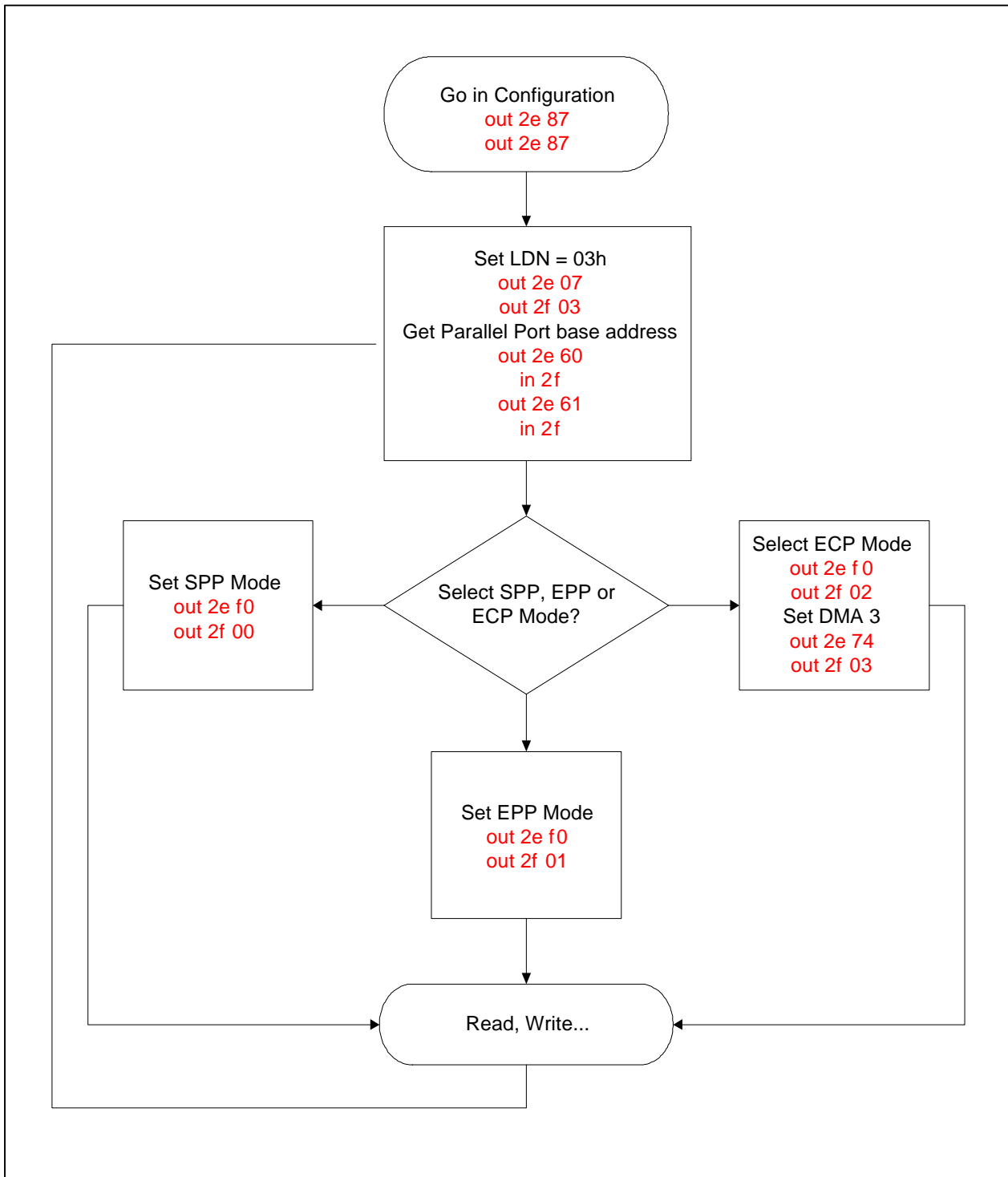
Figure 4-6. Select Parallel Port Modes Flow Chart

4.6   SWC (LDN=04h)

Table 4-9. SWC Configuration Registers

LDN	Index	R/W	Power-Well	Default	Configuration Register or Action
04h	E0h	R/W	VSB	--	SWC Status Register 1
04h	E1h	R/W	VSB	--	SWC Status Register 2
04h	E2h	R/W	VSB	00h	SWC_STS1 to PME during VCC ON Enable Register
04h	E3h	R/W	VSB	00h	SWC_STS2 to PME during VCC ON Enable Register
04h	E4h	R/W	VSB	00h	SWC_STS1 to PME during VCC OFF Enable Register
04h	E5h	R/W	VSB	00h	SWC_STS1 to SMI during VCC ON Enable Register
04h	E6h	R/W	VSB	00h	SWC_STS2 to SMI during VCC ON Enable Register
04h	E7h	R/W	VSB	00h	SWC_STS1 to SMI during VCC OFF Enable Register
04h	F0h	R/W	VPP[Note]	00h	Power ON Event Enable Register
04h	F1h	R/W	VSB	00h	Power ON Status Register
04h	F2h	R/W	VPP[Note]	00h	Power ON Control Register
04h	F3h	R/W	VPP[Note]	00h	Reserved
04h	F4h	R/W	VPP[Note]	00h	SWC Miscellaneous Control Register
04h	F5h	R/W	VPP[Note]	-	SWC Special Code Index Register
04h	F6h	R/W	VPP[Note]	-	SWC Special Code Data Register

Note: VPP is supported by VSB when VSB is present, and is supported by VBAT when VSB is not present.

4.7   Keyboard (LDN=05h)

Table 4-10. Keyboard Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
05h	30h	R/W	00h or 01h	Keyboard Activate
05h	60h	R/W	00h	KBC Data Base Address MSB Register
05h	61h	R/W	60h	KBC Data Base Address LSB Register
05h	62h	R/W	00h	KBC Command Base Address MSB Register
05h	63h	R/W	64h	KBC Command Base Address LSB Register
05h	70h	R/W	01h	Keyboard Interrupt Level Select
05h	71h	RO-R/W	02h	Keyboard Interrupt Type [Note]
05h	F0h	R/W	00h	KBC Special Configuration Register

Note: The register is **read only** unless the write enable bit (Index=F0h) is asserted.

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Table 4-11. Data Register READ/WRITE Controls

Host Address [Note]	R/W*	Function
60h	RO	READ DATA
60h	WO	WRITE DATA, (Clear F1)
64h	RO	READ Status
64h	WO	WRITE Command, (set F1)

Table 4-12. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF
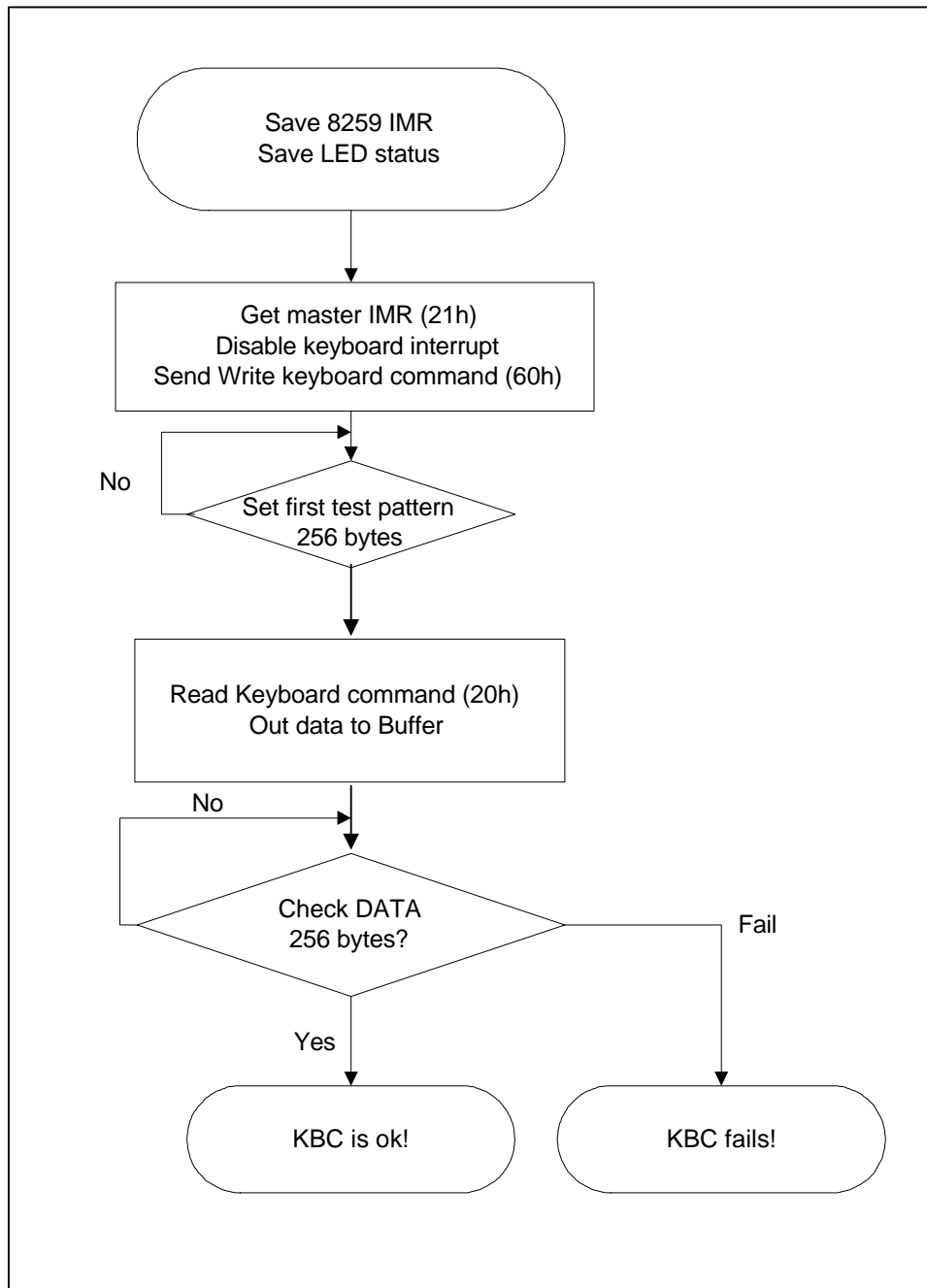
Figure 4-7. KBC Command Byte Register Test Flow Chart

4.8   Game Port (LDN=08h)

Table 4-13. Game Port Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
08h	30h	R/W	00h	Game Port Activate
08h	60h	R/W	02h	Game Port Base Address MSB Register
08h	61h	R/W	01h	Game Port Base Address LSB Register

GAME PORT REGISTERS

R/W

Bit 7 — B - #2 Button
Bit 6 — B - #1 Button
Bit 5 — A - #2 Button

Digital Input

Bit 4 — B - #1 Button
Bit 3 — B - Y Coordinate
Bit 2 — B - X Coordinate

Resistive Input

Bit 1 — A - Y Coordinate
Bit 0 — A - X Coordinate
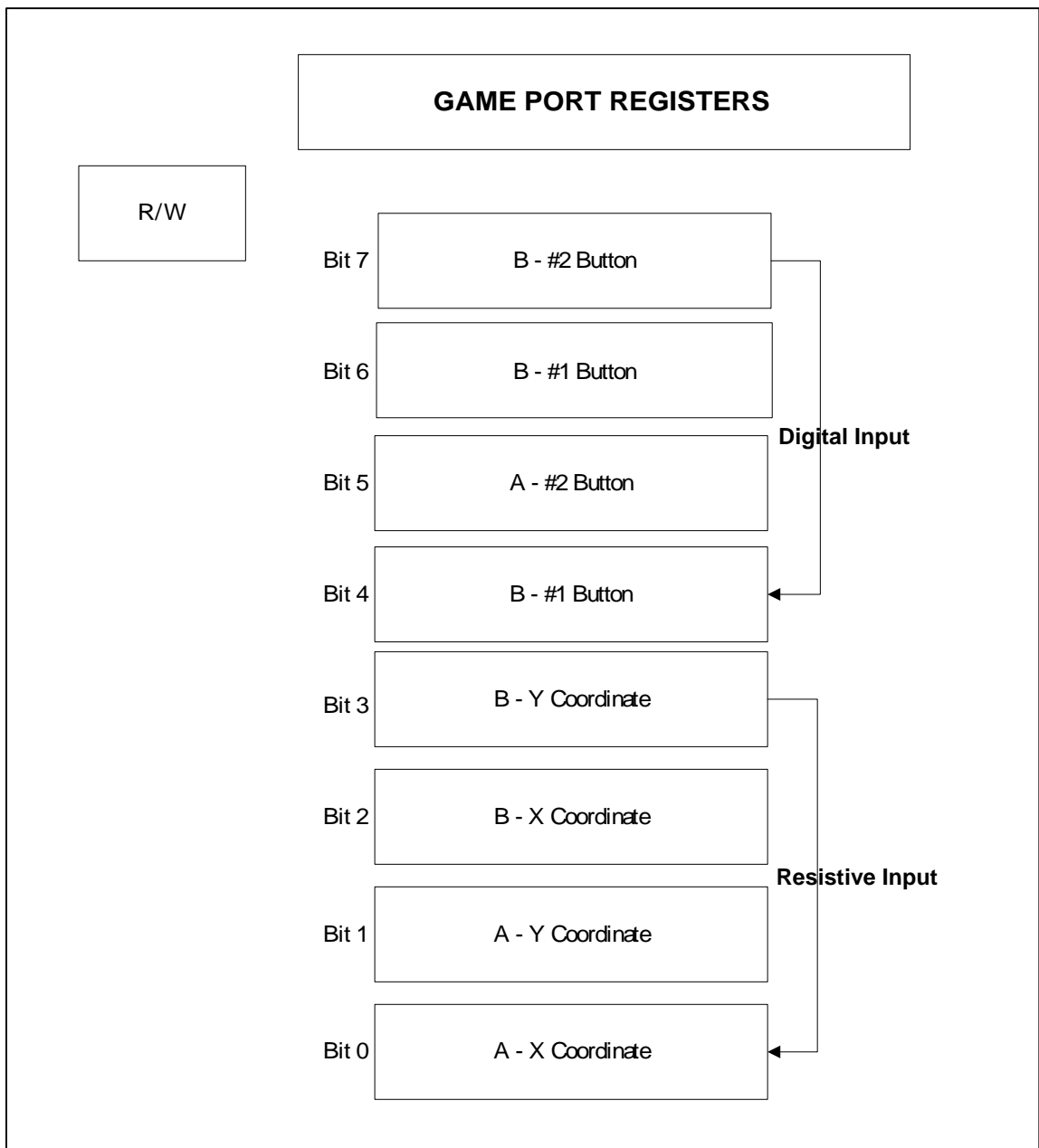
Figure 4-8. Game Port Register

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```
            ╭─────────────────────────╮
            │   Go in Configuration   │
            │       out 2e 87         │
            │       out 2e 87         │
            ╰─────────────────────────╯
                         │
                         ▼
            ┌─────────────────────────┐
            │     Set LDN = 08h       │
            │       out 2e 07         │
            │       out 2f 08         │
            │ Get Game Port base address │
            │       out 2e 60         │
            │         in 2 f          │
            │       out 2e 61         │
            │         in 2 f          │
            └─────────────────────────┘
                         │
                         ▼
            ┌─────────────────────────┐
            │  Send Game Port Message │◄──┐
            └─────────────────────────┘   │
                         │                 │
                         ▼                 │
            ╭─────────────────────────╮   │
            │      Input, Output      │───┘
            ╰─────────────────────────╯
```
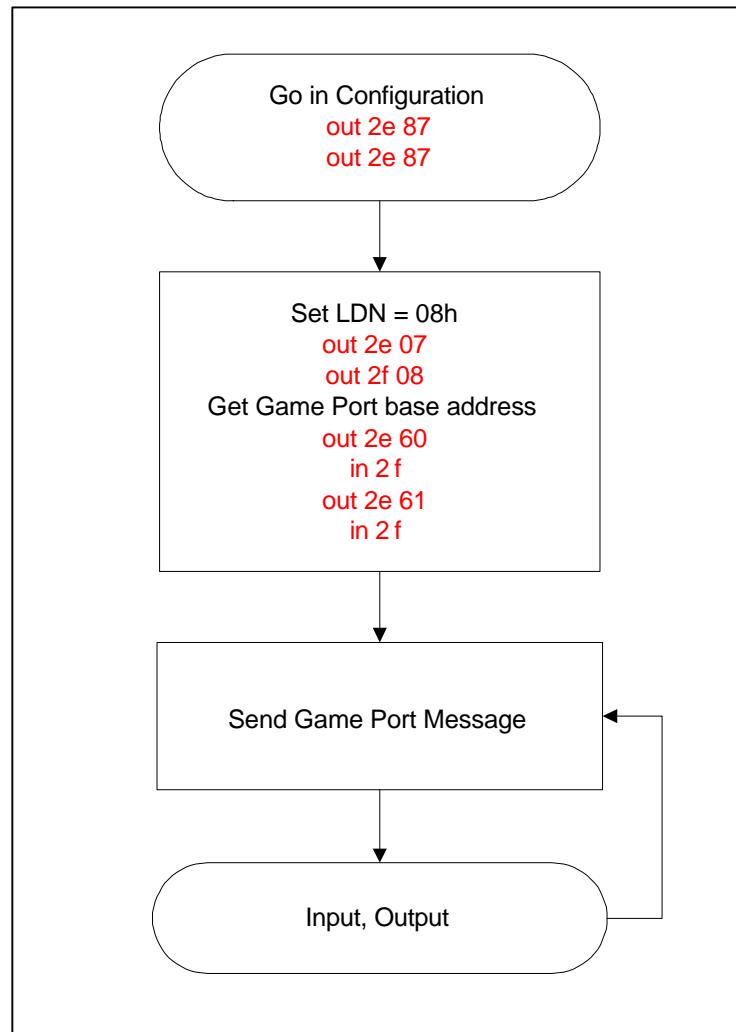
Figure 4-9. Game Port I/O Flow Chart

The Game port integrates four timers for two joysticks. The IT8711F allows the Game Port base address to be located within the host I/O address space 100h to 0FFFh. Currently, most game software assume that the Game (or Joystick) I/O port is located at 201h.

A write to the Game port base address will trigger four timers. A read from the same address returns four bits that correspond to the output from the four timers, and other four status bits corresponding to the joystick buttons will also be returned. A button value of 0 indicates that the button is pressed. When the Game port base address is written, the X/Y timer bits go high. Once the Game port base address is written, each timer output remains high for a duration of time determined by the current joystick position.

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4.8.1 Game Port (Base+0h)

Bit	Signal	Description
7	JBB2	**Joystick B, Button 2 (pin 56 of Joystick connector)**
6	JBB1	**Joystick B, Button 1 (pin 55 of Joystick connector)**
5	JBCY	**Joystick B, Coordinate Y (pin 54 of Joystick connector)**
4	JBCX	**Joystick B, Coordinate X (pin 53 of Joystick connector)**
3	JAB2	**Joystick A, Button 2 (pin 52 of Joystick connector)**
2	JAB1	**Joystick A, Button 1 (pin 51 of Joystick connector)**
1	JACY	**Joystick A, Coordinate Y (pin 50 of Joystick connector)**
0	JACX	**Joystick A, Coordinate X (pin 49 of Joystick connector)**

4.9 CIR (LDN=09h)

Table 4-14. Consumer IR Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
09h	30h	R/W	00h	Consumer IR Activate
09h	60h	R/W	03h	Consumer IR Base Address MSB Register
09h	61h	R/W	10h	Consumer IR Base Address LSB Register
09h	70h	R/W	0Bh	Consumer IR Interrupt Level Select
09h	F0h	R/W	00h	Consumer IR Special Configuration Register

a. Set CIR Registers:

TX: baud rate, frequency, pulse width, pulse mode, deferral mode, RLE mode and FIFO threshold.
RX: Baud rate frequency range, sync mode and FIFO threshold.

b. Begin to Transmit/Receive Data:

TX: Before transmitting any data, the TX FIFO must be cleared first. The device then starts to transmit one frame data into the FIFO. During data transmit, the TX FIFO byte count must be monitored closely to ensure the byte count is remained below the maximum FIFO value, for FIFO to receive further data. It is recommended to clear the FIFO data before the next frame data transmission can be started.

RX: Before transmitting any data, the RX FIFO must be cleared first. RXEN and RXEND are then enabled, and RXACT is asserted low by writing 1 to clear this bit, as illustrated in the diagram on the next page.
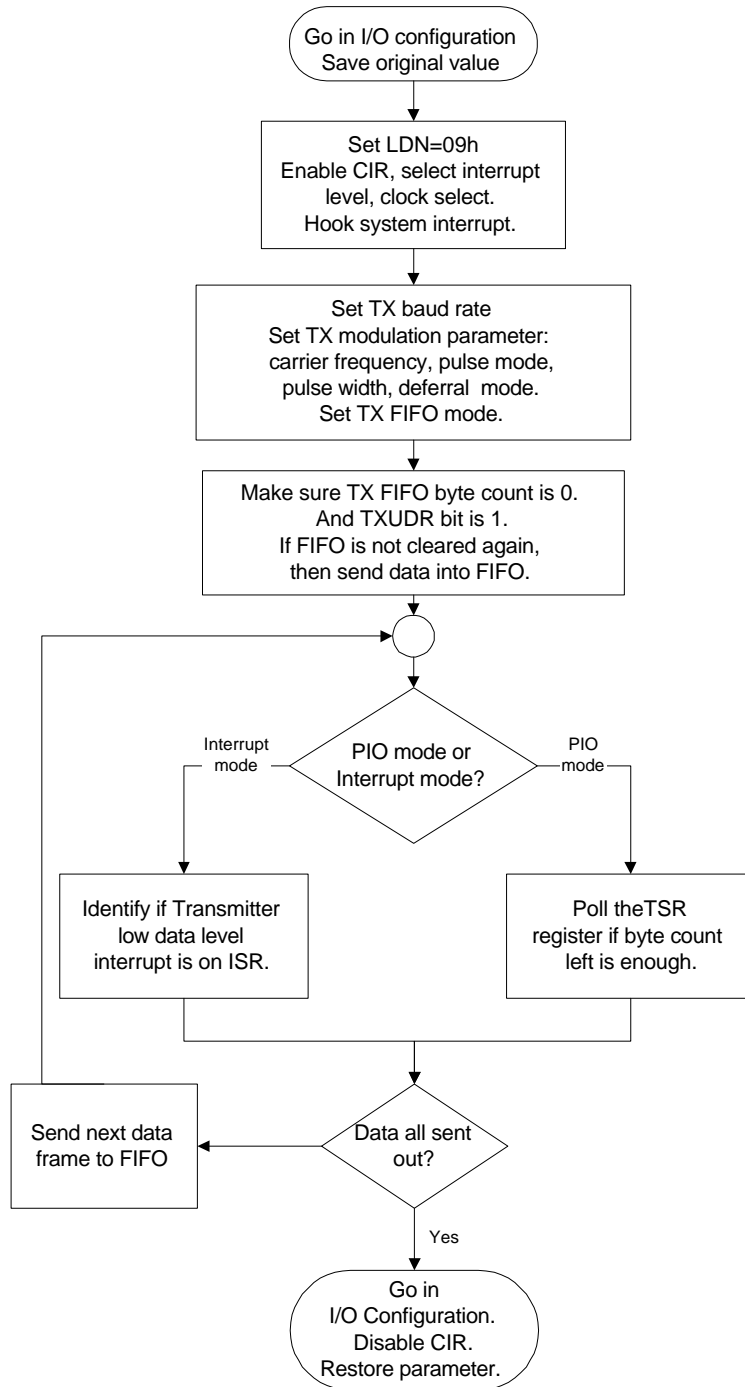
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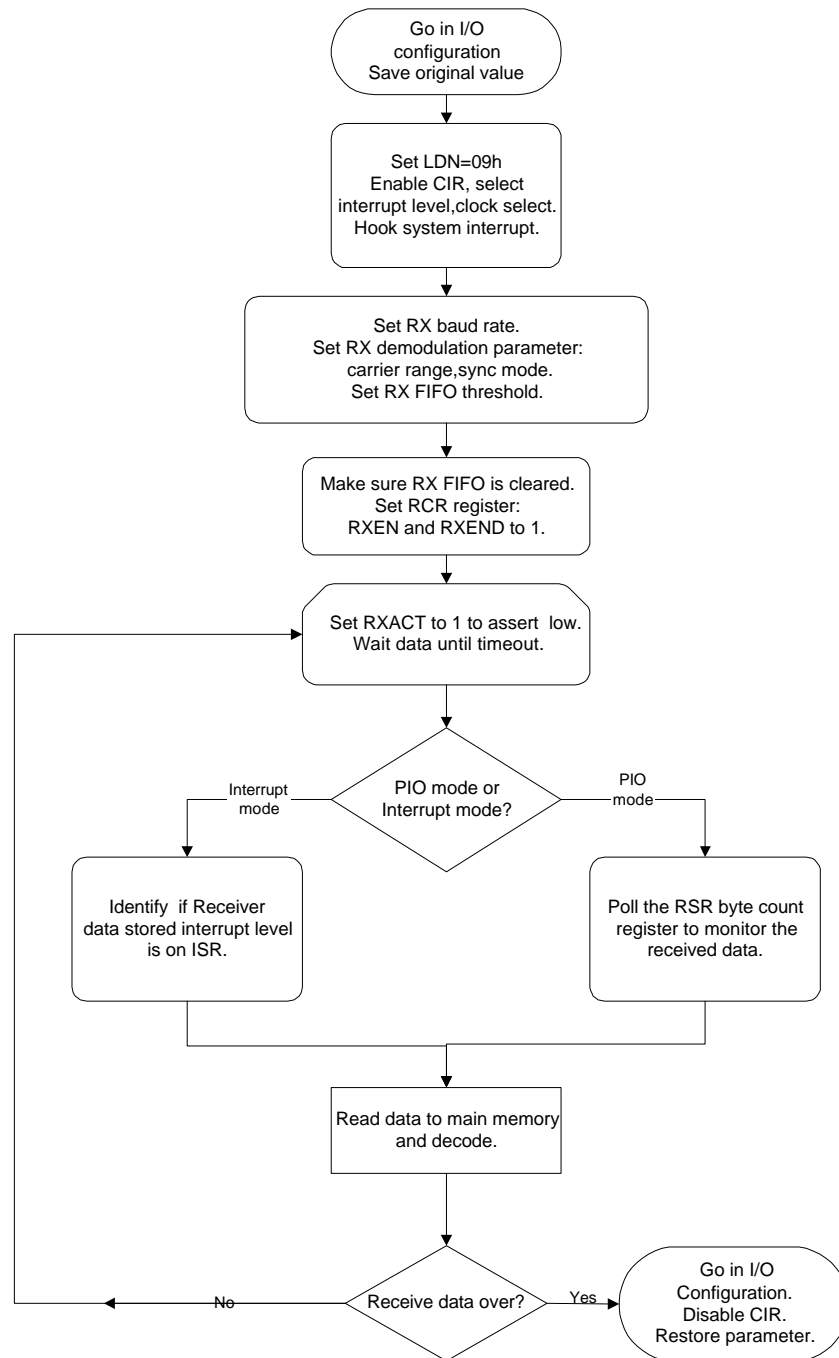
Figure 4-10. CIR RX Flow Chart

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Figure 4-11. CIR TX Flow Chart

4.10   MIDI (LDN=0Ah)

Table 4-15. MIDI Port Configuration Registers

LDN	Index	R/W	Default	Configuration Register or Action
0Ah	30h	R/W	00h	MIDI Port Activate
0Ah	60h	R/W	03h	MIDI Port Base Address MSB Register
0Ah	61h	R/W	00h	MIDI Port Base Address LSB Register
0Ah	70h	R/W	0Ah	MIDI Port Interrupt Level Select
0Ah	F0h	R/W	00h	MIDI Port Special Configuration Register

The IT8711F supports the MIDI capability by incorporating hardware to emulate the MPU-401 in the UART mode. It is software compatible with MPU-401 interface, but only supports the **UART mode** (non-intelligent mode). The UART is used to convert parallel data to the serial data required by MIDI. The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit. The serial data rate is fixed at 31.25 Kbaud.
The MPU-401 logical device occupies two consecutive I/O spaces. The device also uses an interrupt. Both the base address and the interrupt level are programmable. MIDI Base+0 is the MIDI Data port, and MIDI Base+ 1 is the Command/Status port.

MIDI Data Port:
The MIDI Data Port is used to transmit and receive MIDI data. When in UART mode, all transmit data is transferred through a 16-byte FIFO and receive data through another 16-byte FIFO.

UART Mode:

1.   All reads of the Data port, MIDI Base+0, return the next byte in the receive buffer FIFO. The serial data received from the MIDI_IN pin is stored in the receive buffer FIFO. The bit 7 RXS of the Status register is updated to reflect the new receive buffer FIFO status. The receive data available interrupt will be issued only if the FIFO has reached its programmed trigger level. The interrupts will be cleared as soon as the FIFO drops below its trigger level. The trigger level is programmable by changing bits 2-1 of the MIDI port Special Configuration Register, LDN8_F0h.

2.   All writes to the Data port, MIDI Base+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the data bytes are read from the buffer in turn and sent out from the MIDI_OUT pin. The bit 6 TXS of the Status Register is updated to reflect the new transmit buffer FIFO status.

3.   All writes to the Command port, MIDI Base+1, are monitored and acknowledged below:

FFh: Set the interface into the initialization condition. The interface returns to the intelligent mode
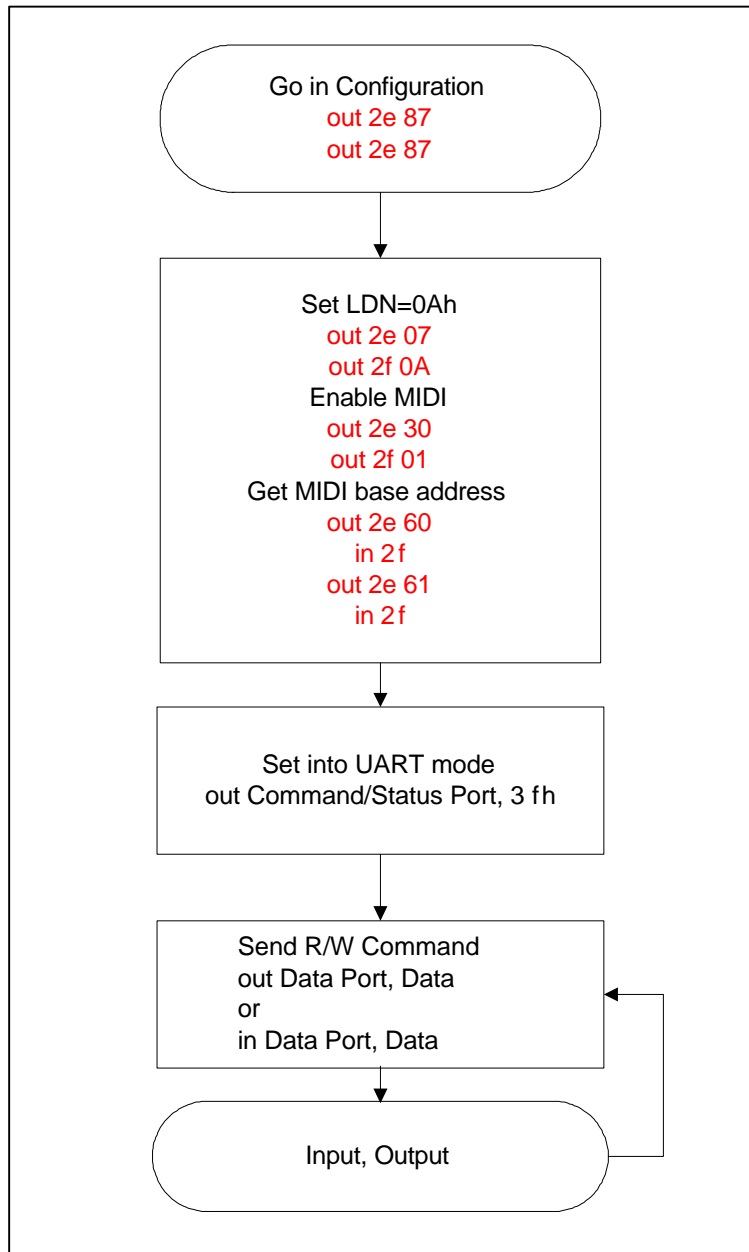**Others:** No operation

Figure 4-12. MIDI I/O Flow Chart

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